APPLICATION NOTE

ABSTRACT
Philips Semiconductors' PDI1394P21/P23/P25 1394 physical layer devices are designed to be pin and function compatible to Texas Instruments' TSB41LVxx and TSB41ABx physical layer devices. This application note outlines considerations that designers need to take into account when creating a dual source socket.

AN2454

Philips Semiconductors' PDI1394P21/P23/P25 second source design considerations

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AN2454

1. INTRODUCTION

The PDI1394P21/P23/P25 physical layer devices are designed to be pin and function compatible to Texas Instruments TSB41LV03A/AB3, TSB41LV02A/AB2, and TSB41LV01/AB1 (respectively) physical layer devices. Even though the P2x devices were designed to be pin and function compatible to the TI devices, some considerations need to be taken by the designer if he/she wishes to have a true second source between Philips and TI. Table 1 shows a matrix of Philips Semiconductors' P21/P23/P25 physical layer devices and their associated pin compatible devices.

Table 1. PDI1394P2x family selection guide

Feature	PDI1394P21	PDI1394P23	PDI1394P25
Speed	400	400	400
No. Of Ports	3	2	1
IEEE1394-compliant	IEEE1394a-2000	IEEE1394a-2000	IEEE1394a-2000
Power supply	3.3 V (5 V tolerant I/O)	3.3 V (5 V tolerant I/O)	3.3 V (5 V tolerant I/O)
Supply current in power-down mode	150 µA	150 µA	150 µA
Additional features	P21 requires fewer external components than TI devices	P23 can be configured as a 1 port Phy with no extra external components	Requires fewer external components than TI devices
Availability	Samples – Now Production – Q3 '01	Samples – Now Production – Q2 '01 (P23)	Samples – Now Production – Q2 '01
Package	LQFP80	LQFP64	LQFP64
Pin compatibility	TI TSB41LV03x/ TSB41AB3	TI TSB41LV02x/ TSB41AB2	TI TSB41LV01/ TSB41AB1*

* 64-pin package.

2. BOARD DESIGN CONSIDERATIONS

The Philips Semiconductors P21, P23, and P25 devices were designed to be drop in replacements to the TI TSB41LV03, TSB41LV03A, TSB41AB3, TSB41LV02, TSB41LV02A, TSB41AB2, TSB41LV01, and TSB41AB1 (Table 1 illustrates which Philips devices are compatible to which TI devices). Even though the Philips devices where designed to be drop in compatible to the TI devices, the TI devices are **not** drop in compatible to the Philips' devices. The TI devices require more external components than the Philips devices require. These extra external components required by the TI physical layer devices have no adverse affects to the Philips Physical Layer devices. This section explains these differences and it is left up to the developer to decide which board design best meets their project objectives.

2.1. PDI1394P21 and TSD41LV03A/AB3 design differences

2.1.1. Pin 9 (LV03A/AB3 = V_{DD} – 5 V; P21 = NC)

1. **LV03A/AB3:** This pin should be connected to the LLC (Link Layer Controller) V_{DD} supply when a 5 V LLC is used and should be connected to the PHY DV_{DD} when a 3 V LLC is used. A combination of high-frequency decoupling capacitors near this terminal is suggested, such as paralleled 0.1 μF and 0.001 μF. When this terminal is tied to a 5 V supply, all terminal bus holders are disabled, regardless of the state of the ISO (Link Interface Isolation Control Input) terminal. When this terminal is tied to a 3 V supply, bus holders are enabled when the ISO terminal is high.

2. **P21:** Since this pin is a no connect (which has no internal connections to the die), applying power to this pin as required by the LV03A/AB3 will have no affect to the operation of the P21.

2.1.2. Pin 31 (LV03A/AB3 = TESTM; P21 = NC)

Test Control input

1. **LV03A/AB3:** This pin is used in the manufacturing test of the TSB41LV03A/TSB41AB3; for normal use this terminal should be tied to V_{DD}.

2. **P21:** Since this pin is a no connect (which has no internal connections to the die) applying V_{DD} to this pin as required by the LV03A/AB3 will have no affect to the operation of the P21.

2.1.3. Pin 32 (LV03A/AB3 = SE; P21 = TEST1)

Test Control input

1. **LV03A/AB3:** This pin is used in manufacturing test, for normal use this terminal should be tied to GND through a 1 kΩ pull-down resistor.

2. **P21:** For normal use this pin should be tied directly to GND, but the P21 will operate correctly if this pin is pulled to GND through a 1 kΩ resistor as required by the LV03A/AB3.

2.1.4. Pins 71 and 72 (LV03A/AB3 = FILTER0, FILTER1; P21 = NC)

I/O PLL filter terminals

1. **LV03A/AB3:** These terminals are connected to an external capacitor to form a lag-lead filter required for stable operation of the internal frequency-multiplier PLL running off of the crystal oscillator. A 0.1 μF ± 10% capacitor is the only external component required to complete this filter.

2. **P21:** The P21 does not require an external capacitor on these pins for stable operation. On the P21 these pins are no connects (which have no internal connections) thus the device will work properly with or without the external capacitor.

2.2. 3 port design schematics

This section highlights the recommended designs for the PDI1394P21 and TSB41LV03A/TSB41AB3 devices. These designs are for reference only and the designer should refer to the appropriate vendor data sheet for further details on designing the part into their design.

Figure 1 represents a "typical" Philips P21 Physical Layer design. Figure 2 represents a TI TSB41LV03A and TSB41AB3 design in the same "typical" scenario as the P21 design shown in Figure 1. The represented designs are referred to as typical because they can be used in a wide variety of designs with few changes.

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AN2454

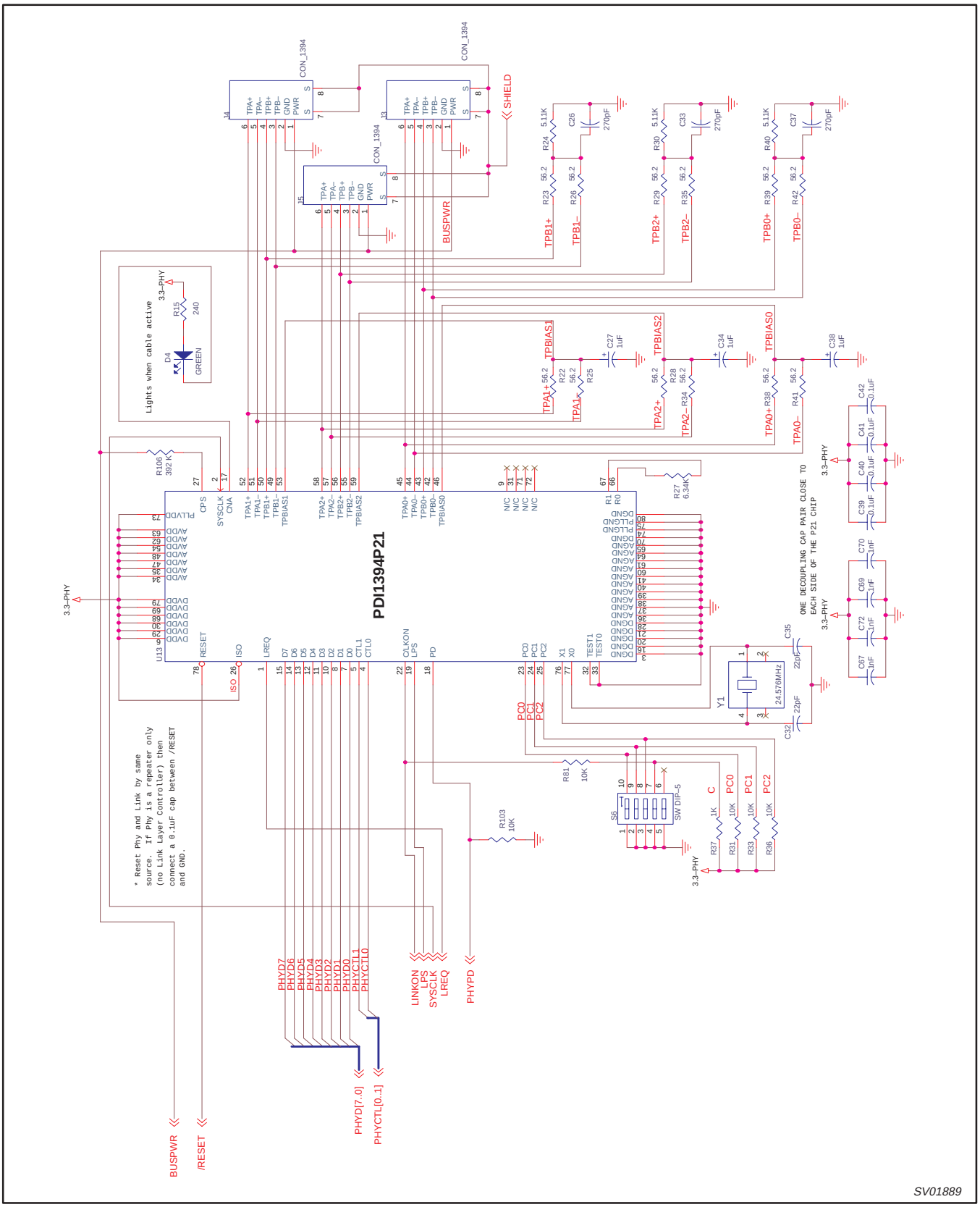

Figure 1. Typical P21 three port PHY design.

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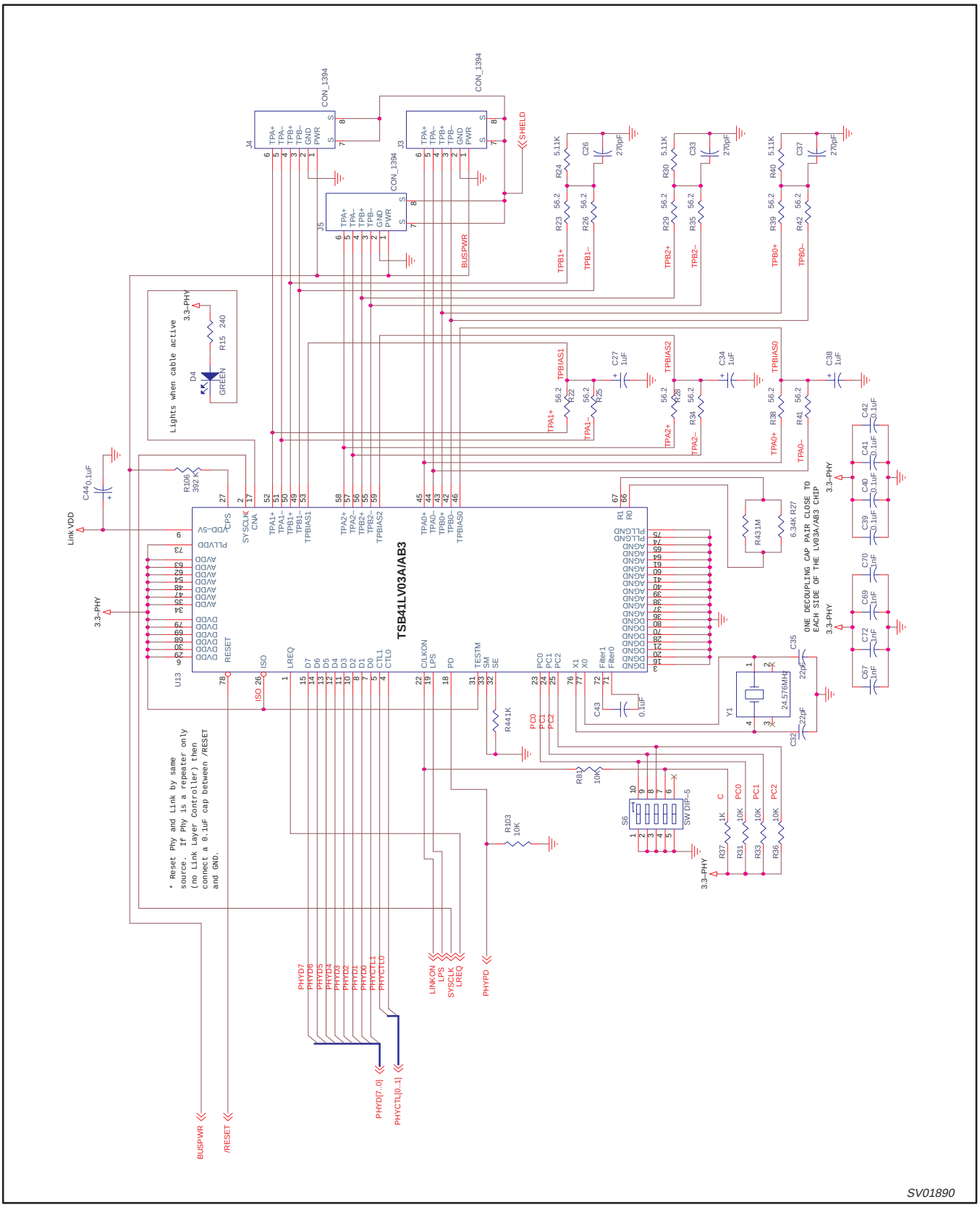

Figure 2. Typical LV03A/AB3 three port PHY design.

2.3. PDI1394P23 and TSB41LV02A/AB2 design differences

2.3.1. Pin 27 (LV02A/AB2 = TESTM; P23 = TWOPORT)

Test Control input

1. **LV02A/AB2:** This pin is used in the manufacturing test of the TSB41LV02A/TSB41AB2; for normal use this terminal should be tied to V_{DD}.

2. **P23:** This pin is used to select between one and two port operation. When this pin is tied to V_{DD} (as required by the LV02A/AB2) both ports 0 and 1 are enabled. When this pin is tied to GND, port 1 is disabled and port 0 is enabled.

2.3.2. Pin 28 (LV02A/AB2 = SE; P23 = BRIDGE)

Test Control input

1. **LV02A/AB2:** This pin is used in the manufacturing test, for normal use this terminal should be tied to GND through a 1 kΩ pull-down resistor.

2. **P23:** This pin is used to set the Bridge_Aware bits located in the Vendor-Dependent register Page 7, base address 1001_b. When this pin is tied low (either directly to GND or through a 1 kΩ resistor as required on the LV02A/AB2) the Bridge_Aware bits are set to 00_b indicating this node is a non-bridge node. When this pin is tied high, the Bridge_Aware bits are set to 11_b, indicating this node is a 1394.1 bridge compliant node. For more information on the functionality of this field, please refer to the P23 datasheet and the 1394.1 specification.

2.3.3. Pins 54 and 55 (LV02A/AB2 = FILTER0, FILTER1; P23 = NC)

I/O PLL filter terminals

1. **LV02A/AB2:** These terminals are connected to an external capacitor to form a lag-lead filter required for stable operation of the internal frequency-multiplier PLL running off of the crystal oscillator. A 0.1 µF ± 10% capacitor is the only external component required to complete this filter.

2. **P23:** The P23 does not require an external capacitor on these pins for stable operation. On the P23 these pins are no connects (which have no internal connections), thus the device will work properly with or without the external capacitor.

2.4. 2 port design schematics

This section highlights the recommended designs for the PDI1394P23 and TSB41LV02A/TSB41AB2 devices. These designs are for reference only and the designer should refer to the appropriate vendor datasheet for further details on designing the part into their design.

Figure 3 represents a "typical" Philips P23 Physical Layer design. Figure 4 represents a TI TSB41LV02A and TSB41AB2 design in the same "typical" scenario as the P23 design shown in Figure 3. The represented designs are referred to as typical because they can be used in a wide variety of designs with few changes.

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AN2454

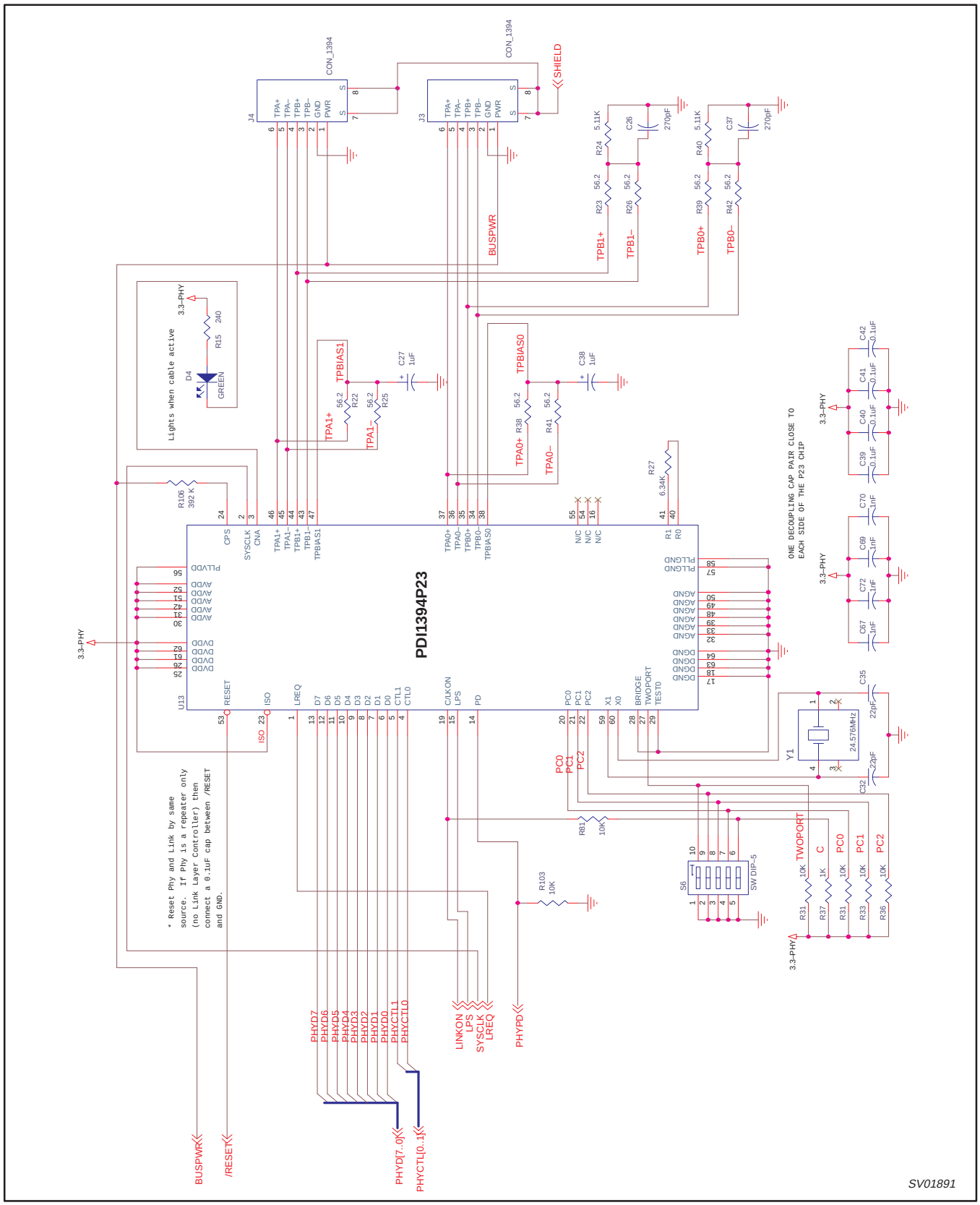

Figure 3. Typical P23 two port PHY design.

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AN2454

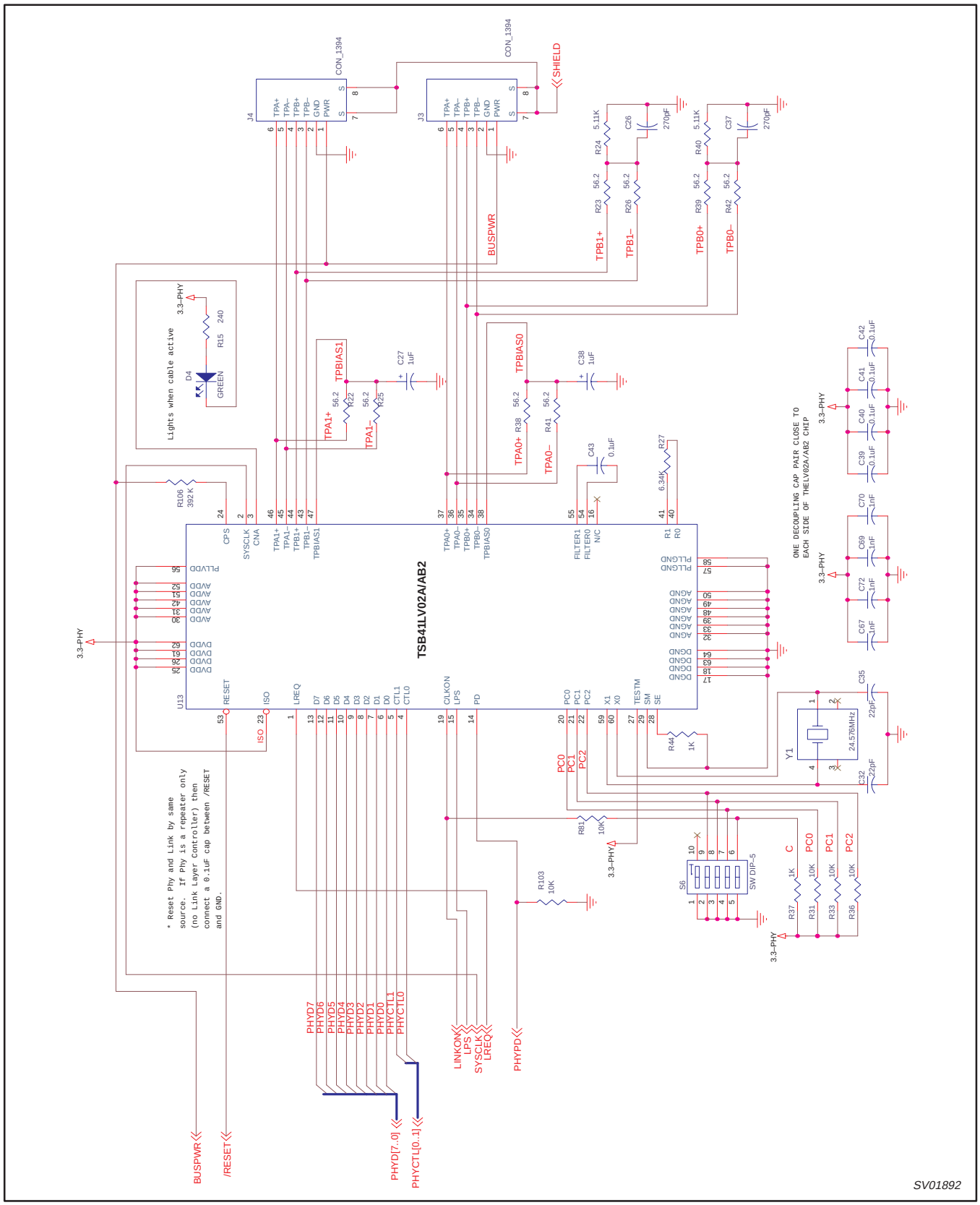

Figure 4. Typical LV02A/AB2 two port PHY design.

2.5. PDI1394P25 and TSB41LV01/AB1 design differences

The TSB41LV01 is available in a 64-pin package, and the TSB41AB1 is available in both a 48-pin package and a 64-pin package. The PDI1394P25 is pin and function compatible to the 64-pin devices only.

2.5.1. Pin 28 (LV01/AB1 = SE; P25 = TEST1)

Test Control input

1. **LV01/AB1:** This pin is used in the manufacturing test, for normal use this terminal should be tied to GND through a 1 kΩ pull-down resistor.
2. **P25:** For normal use, this pin should be tied directly to GND, but the P25 will operate correctly if this pin is pulled to GND through a 1 kΩ resistor as required by the LV01/AB1.

2.5.2. Pins 54 and 55 (LV01/AB1 = FILTER0, FILTER1; P25 = NC)

I/O PLL filter terminals

1. **LV01/AB1:** These terminals are connected to an external capacitor to form a lag-lead filter required for stable operation of the internal frequency-multiplier PLL running off of the crystal oscillator. A 0.1 µF ± 10% capacitor is the only external component required to complete this filter.
2. **P25:** The P25 does not require an external capacitor on these pins for stable operation. On the P25 these pins are no connects (which have no internal connections), thus the device will work properly with or without the external capacitor.

2.6. 1 port design schematics

This section highlights the recommended designs for the PDI1394P25 and TSB41LV01/TSB41AB1 devices. These designs are for reference only, and the designer should refer to the appropriate vendor data sheet for further details on designing the part into their design.

Figure 5 represents a "typical" Philips P25 Physical Layer design. Figure 6 represents a TI TSB41LV01 and TSB41AB1 design in the same "typical" scenario as the P25 design shown in Figure 5. The represented designs are referred to as typical because they can be used in a wide variety of designs with few changes.

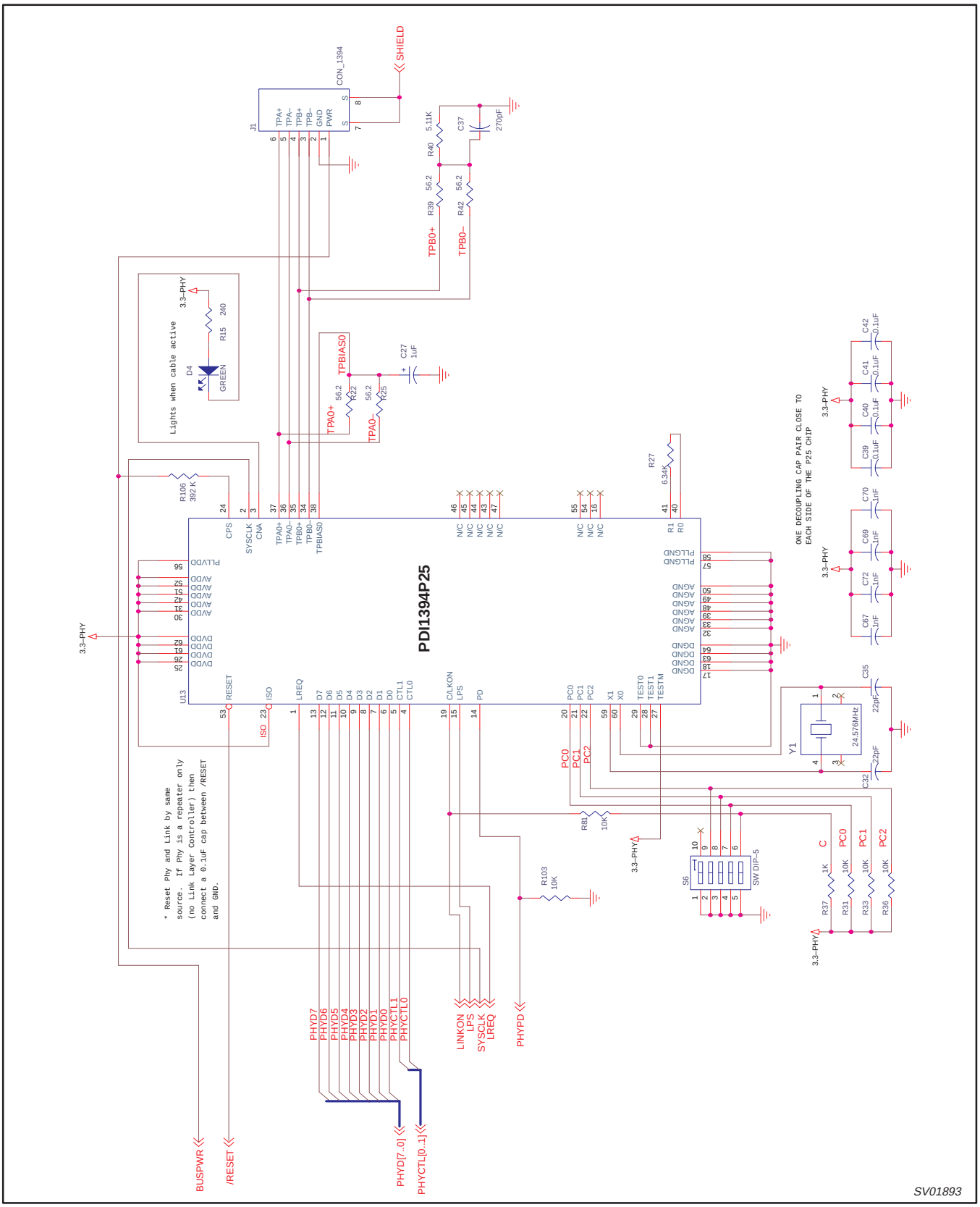

Figure 5. Typical P25 one port PHY design.

Philips Semiconductors' PDI1394P21/P23/P25 second source design considerations

AN2454

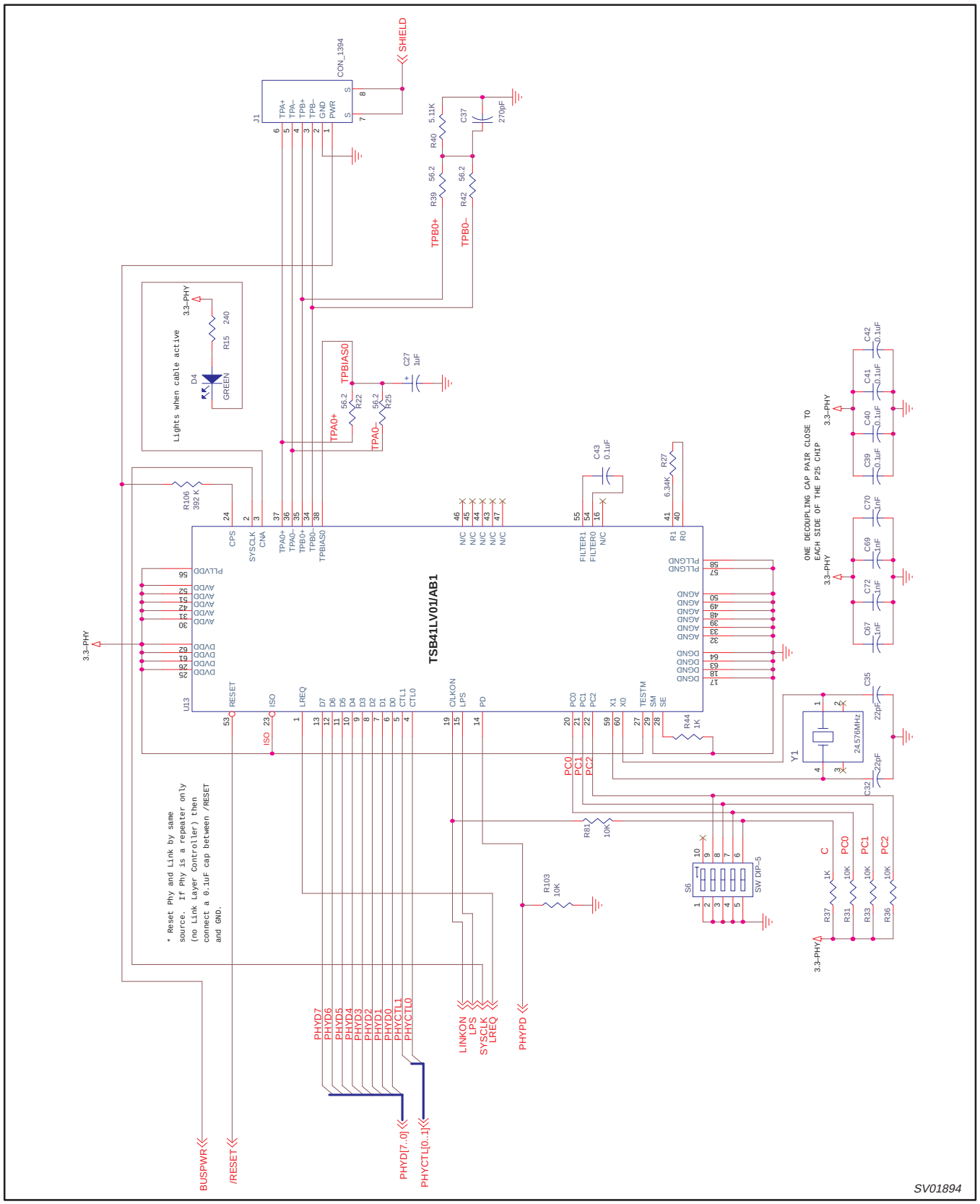

Figure 6. Typical LV01/AB1 one port PHY design.

3. CONTACT INFORMATION

In case of any questions or suggestions regarding this application note or any other related 1394 issues, please feel free to contact the Philips 1394 Applications and Marketing group at **1394@philips.com**.
For information on Philips Semiconductors' 1394 chipsets and tools, please visit our web site at **www.semiconductors.philips.com/1394**.

4. REFERENCES

- PDI1394P21 data sheet
- PDI1394P23 data sheet
- PDI1394P25 data sheet
- TSB41LV01 data sheet (available from Texas Instruments)
- TSB41AB1 data sheet (available from Texas Instruments)
- TSB41LV02A data sheet (available from Texas Instruments)
- TSB41AB2 data sheet (available from Texas Instruments)
- TSB41LV03A data sheet (available from Texas Instruments)
- TSB41AB3 data sheet (available from Texas Instruments)
- *Fire Wire System Architecture*, Second Edition; Don Anderson; MindShare, Inc.; 1999; ISBN 0-201-48535-4.
- 1394 Trade Association Website: **http://www.1394ta.org/**

NOTES

Philips Semiconductors' PDI1394P21/P23/P25 second source design considerations

AN2454

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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